

## Bluetooth™ Module UGXZ5 Specification

Model number	Function	Specification revision	Remarks
UGXZ5-603A	Output Power class1 compliant SMD (solder ball bump array) Flash memory, Reference oscillator built in UART (RAW), PCM interfaces	spec. 1.1.0	

Digit	Definition	Contents
Digit 0~3	Bluetooth™ Module Including Base Band	UGXZ
Digit 4	Output Power class	5: Class1-HCI module, voltage regulator built in
Digit 5	Status of products	X: Engineering Sample -: Mass production
Digit 6	Interface dependent	6 : UART (RAW : 115.2kbps)
Digit 7~8	Serial number	03 : for ALEU
Digit 9	Revision	Starting from A

**CONFIDENTIALITY NOTES:**

This specification contains confidential information, which shall not be provided to any third parties without agreement notice.

**CAUTION**

1.The BLUETOOTH trademarks are owned by Bluetooth SIG, Inc., U.S.A.

2.The Bluetooth™ Module contains capability to upgrade own firmware via USB or UART interface. This feature can be used for development purpose only. Firmware upgrade by end user in the market may be restricted by regulatory rule depending on each country. ALPS will not own any responsibilities of infringement of each country's regulatory law for firmware upgrade.

3. This product (or technology) is controlled item subject to the Japanese Foreign Exchange and Foreign Trade Law. It should not be exported from Japan without authorization from the appropriate governmental authorities.

4. ALPS guarantees performance only for the standard configuration (PS\_KEY settings). In case of any modifications on PS\_KEY settings by customer, the original guarantee will no longer be applied. If there is any objections on product quality, all analysis on the module performances will be done based only on ALPS standard configuration (PS\_KEY setting).

**BLUETOOTH™ MODULE UGXZ5 SPECIFICATION****1 GENERAL**

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**1 GENERAL****1-1 Purpose and Scope of this document**

This document contains the specifications pertinent to the module for Bluetooth™ system, which comply with BLUETOOTH™ Specifications Version 1.2.

This document specifies and describes General, Mechanical, Electrical, Software and Reliability specifications and aspects for ALPS Bluetooth™ Module ver2.9.

**1-2 Product Overview**

ALPS Bluetooth™ Module contains CSR BC2-EXT (BC212015), which has complete radio part and base band controller section (16bits RISC processor, RAM and Flash memory). Also, high accuracy reference oscillator and sub clock for extremely low power management are built in. Protocol software is already downloaded into integrated Flash memory and interfaces to HCI layer of upper layer protocol stack on an appropriate host system.

ALPS Bluetooth™ Module permits standard operating conditions according to the following table and will perform typical features described on the second table.

**1-2-1 Standard Operating Conditions**

Items	Conditions
Operating Temperature	Nominal: +15 °C to +35 °C Extreme: -20°C to +75 °C
Operable Temperature	-20°C to +75 °C
Storage Temperature	-30 °C to +85 °C
Supply Voltage; VCC	Nominal: +3.3 V Extreme: +3.3 V ± 0.1 V
Absolute Maximum Ratings Supply Voltage	VCC: -0.4V ~ +3.6V

**1-2-2 Features List**

Features	Contents
Power level	+12.5 dBm typ.
Program memory	8M bits Flash
RAM	32k bytes x 16 bits
Reference oscillator	Built in
Sub clock oscillator	Built in
Audio interface	PCM A-Law, $\mu$ -Law (CVSD)
Serial data interface	UART (RAW : 115.2 kbps)
Physical connection	SMD (solder ball bump array)

**1-3 Radio part**

Bluetooth™ Module has fully integrated 2.4GHz radio transceiver with Class1 power amplifier, receiver and frequency-hopping synthesizer. In order to facilitate power management, each section of the radio may be powered up and down separately. Various software controllable switches have been implemented to control power to the transmitter, the frequency synthesizer/VCO, the receiver and the LNA.

**1-4 Base band part**

Bluetooth™ Module contains link controller, which performs all the real-time functions of the Bluetooth™ baseband protocol layer, including data transfer and connection management. The device also controls states of operation enables sniff, park and hold modes of operation. Real-time functions such as frequency-hopping burst timing and clock synchronization are also implemented in this hardware. Further processing is required to format the data into the Bluetooth™ packet format before it may be applied to the GFSK modulator. On the receive side the controller performs error correction and de-scrambling before de-packet zing the incoming payload and storing it in RX buffers.

The link controller hardware also implements the basic, repetitive actions of paging, inquiry, page or inquiry scans and the general Bluetooth™ modes of park and sniff. This ensures that the processor used to implement the Link Manager and other lower layer protocol can be kept inactive. Also base band contains the following functionality.

**1-4-1 FEC – Forward Error Correction**

FEC provides the ability to correct any errors, which might have occurred during the transmission of the original data. FEC rate of 1/3, 2/3, and Automatic Repeat Request (ARQ) are implemented.

**1-4-2 Whiten / De-whiten – Scramble/Unscramble**

Whitening/Scramble refers to the addition of randomized data to avoid any undesirable DC bias effects in the transfer of data packets. De-whitening/Unscramble is the reversal of the original process where the original data can be extracted.

**1-4-3 Encrypt/Decrypt – Apply/Remove Encryption**

Encryption is the security feature where keys are used to prevent the access of data to unauthorized sources. This functional block is responsible for the processing of authentication and key management functions required by Bluetooth™

**1-4-4 CRC – Cyclic Redundancy Check**

This is the error detection function implemented to process the CRC field within the payload section of a Bluetooth™ transfer packet. On the receive side, the CRC is checked with the expected value based on algorithms. On the transmit, and proper CRC is generated to and appended to the payload.

**1-4-5 HEC – Header Error Correction**

This is the error correction function implemented dealing with the 8-bit HEC field of the Bluetooth™ packet header as specified in Version 1.2 spec.

**1-5 Attention for FAA (Federal Aviation Administration) compliance**

FAA proposal is to restrict use of any wireless devices during entire flight. This restriction is applied for also Bluetooth™ as well. Customer must implements disable switch of Bluetooth™ functionality by hardware or software. Module contains disable and enable radio over extended HCI commands, which shall be implemented into application software for any products, which might be carried out to airplane.

**1-6 LIFE SUPPORT APPLICATIONS**

This product is not designed for use in life support appliances, devices or systems where malfunction of this product can reasonably be expected to result in personal injury. ALPS customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify ALPS for any damages resulting from such improper use or sale.

## 2 RADIO PART (RF) SPECIFICATIONS

All RF specification items below are specified in accordance with Bluetooth™ RF Test Specification Revision 0.92 dated on 2003-Feb-01 and corresponding Critical Erratum.

### 2-1 Common Physical Layer Specifications

Operating Frequency	2402 MHz to 2480 MHz
Carrier Spacing	1.0 MHz
Channel	79
Duplexing	TDD
Symbol Rate	1 Mbps
Modulation Method	GFSK BbT = 0.5
Reference Oscillator	16MHz (built in)
RF input and output impedance	Nominal 50 ohm

### 2-2 TX Specifications

Items	Spec. limits			Unit	Conditions	
	Min	Typ	Max		Temp.	Volt.
Normal Transmit Power						
Peak power	9.0	12.5	15.0	dBm	Nominal	Nominal
Averaged power	7.0		18.0		Extreme	Extreme
Minimum controlled level			4.0	dBm	Nominal	Nominal
Power control step size	2		8	dB	Nominal	Nominal
Radio Frequency Tolerance	-75		+75	kHz	Extreme	Extreme
Radio Frequency drift						
One slot	-25		+25	kHz	Extreme	Extreme
Three slot	-40		+40	kHz		
Five slot	-40		+40	kHz		
Drift Rate	-20		+20	kHz/50μs		
Peak Deviation						
00001111(df1 <sub>avg</sub> )	±140		±175	kHz	Extreme	Extreme
01010101(df2 <sub>min</sub> )	±115			kHz		
01010101(df2 <sub>avg</sub> /df1 <sub>avg</sub> )	80			%		
Spurious Emission (In Band) *1)						
±500 kHz	-20			dBc	Extreme	Extreme
M-N  = 2			-20	dBm		
*2)  M-N  ≥ 3			-40	dBm		
Spurious Emission (out of Band) *3)						
30 MHz ~ 1 GHz			-36	dBm	Extreme	Extreme
1 GHz ~ 12.75 GHz			-30	dBm		
1.8 GHz ~ 1.9 GHz			-47	dBm		
5.15 GHz ~ 5.3 GHz			-47	dBm		
TX current consumption *4)		200	220	mA	Nominal	Nominal

Notes:

\*1) The transmit power shall be measured in the following conditions.

Frequency offset	Test Condition
± 500 kHz	RBW: 10 kHz, VBW: 30 kHz
M-N  = 2	RBW: 100 kHz, VBW: 300 kHz
M-N  ≥ 3	RBW: 100 kHz, VBW: 300 kHz

M : Transmit channel, N : Measured channel

\*2) Exceptions are allowed in up to three bands of 1MHz width centered on a frequency which is an integer multiple of 1MHz. They must, however, comply with an absolute value of -20dBm.

\*3) The transmit power shall be measured in a 100 kHz bandwidth.

\*4) Based on Normal Transmit Power specified on the above table.

### 2-3 RX Specifications

Items	Spec limits			Unit	Conditions	
	Min	Typ	Max		Temp.	Volt.
Reference Sensitivity Level (BER=0.001)		-78	-70	dBm	Extreme	Extreme
Reference Interference Level *1) BER<=0.1%						
Co-ch interference C/I <sub>co</sub>	11			dB	Nominal	Nominal
Adj. (1 MHz) interference C/I <sub>1MHz</sub>	0			dB		
Adj. (2 MHz) interference C/I <sub>2MHz</sub>	-30			dB		
Adj. (≥3 MHz) interference C/I <sub>3MHz</sub>	-40			dB		
Image Ch interference C/I <sub>image</sub>	-9			dB		
Image Ch interference C/I <sub>image±1MHz</sub>	-20			dB		
Out of Band Blocking *2) BER ≤0.1 %					Nominal	Nominal
30 MHz ~ 2 GHz	-10			dBm		
2 GHz ~ 2.4 GHz	-27			dBm		
2.5 GHz ~ 3 GHz	-27			dBm		
3 GHz ~ 12.75 GHz	-10			dBm		
Intermodulation Characteristics *3) BER ≤ 0.1% Carrier Level: -64 dBm	-39			dBm	Nominal	Nominal
Maximum Usable Level	-20			dBm	Nominal	Nominal
Spurious Emission					Nominal	Nominal
30 MHz ~ 1 GHz			-57	dBm		
1 GHz ~ 12.75 GHz			-47	dBm		
RX current consumption		65	75	mA	Nominal	Nominal

Note \*1) Carrier Signal Level: -67 dBm (Adj. (≥3 MHz), Image)

Carrier Signal Level: -60 dBm (Co-chi, Adj. (1 MHz), Adj. (2 MHz)) Frequencies where the requirements are not met are called spurious response frequencies. Five spurious response frequencies with a distance of ≥2 MHz from the wanted signals are allowed. On these spurious response frequencies a relaxed interference requirement C/I = -17 dB must be met.

Note \*2) Carrier Signal level: -67 dBm

24 exceptions are permitted which are dependent upon the given receive channel frequency and are centered at a frequency which is an integer multiple of 1 MHz. At 19 of those spurious response frequencies a relaxed power level -50 dBm of the interfere may be used to achieve a BER of 0.1 % and at the remaining 5 spurious response frequencies the power level is arbitrary.

Note \*3) Carrier signal level: -64 dBm

A static sine wave signal at f1 with a power level of -39 dBm. A Bluetooth™ module signal at f2 with a power level of -39 dBm. Such that f0 = 2f1 - f2 and f2 - f1 = n\*1 MHz, where n can be 3, 4 or 5. The system must fulfill one of there alternatives.

#### REFERENCE INTERFERENCE SIGNAL DEFINITION

A modulated Interfering signal is defined as:

Modulation = GFSK

Modulation index = 0.32 ±1 %

BT = 0.5 ±1 %

Bit rate 1Mbps ±1 ppm

Modulating data = PRBS15

Frequency Accuracy better than ±1 ppm

**3 BASE BAND SPECIFICATIONS**

**3-1 Program memory**

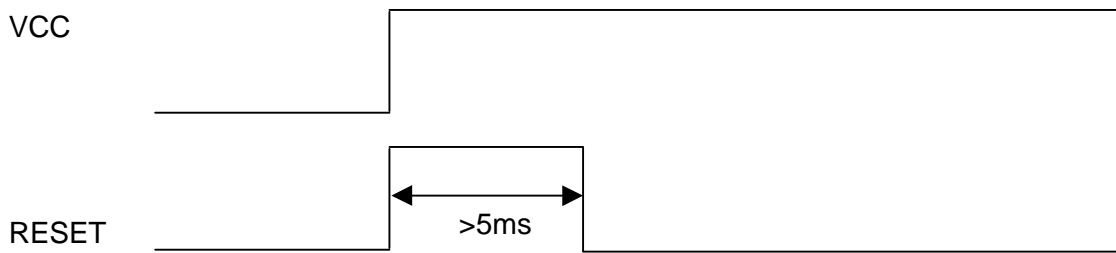
Module contains on chip flash memory that includes Bluetooth™ protocol stack under HCI firmware.

**3-2 Hardware RESET sequence**

When RESET is asserted to module, microprocessor will be initialized.

The reset is positive level triggered based on Schmitt-trigger input and needs a worst case 5ms or wider pulse. Once reset is begun, all I/O ports will be instantly tri-state and stop the clock. The fall-time decay of reset signal can be arbitrarily long. Removal of reset will initiate the system boot, which takes typically several 100ms to reach a state where USB enumeration or UART link establishment can occur.

If the host does not capable of creating such reset signal at the beginning of cold start-up (VCC ramp-up), a 0.22uF capacitor between VCC (pin#2) and RESET (pin#4) is required to maintain module functionality.



**3-3 Physical Interface**

The Bluetooth™ Module contains UART and PCM interfaces. Details of each interface are described on the following sub-chapters.

**3-3-1 UART (Universal Asynchronous Receiver Transmitter)**

Base band processor contains individual transmitter and receiver blocks thus user can use full bi-directional communication. And possible to receive and transmit in continuous by double buffer structure. Host controller can re-configure data format using a private communications logical channel running over the UART. Data bit will be transmitted from LSB as default setting.

UART\_TxD, UART\_RxD, UART\_RTS, UART\_CTS form a conventional asynchronous data serial port. The interface is designed to operate correctly when connected to other UART devices such as the NS16550A. The signaling levels are 0V and VCC. The interface is programmable over a variety of bit rates; no, even or odd parity; one or two stop bits and hardware flow control on or off. The default condition on power-up is pre-assigned in the (external) Flash memory.

The maximum UART data rate is 1.3824Mbps. Two-way hardware flow control is implemented by UART\_RTS and UART\_CTS. UART\_RTS is an output and is active low. UART\_CTS is an input and is active low. These signals operate according to normal industry convention.

**3-3-1-1 Default Data format**

User can set desired data format (software setting should be determined) by the following selection However, Host shall communicate with default setting UART connection initiated at first time.

Baudrate:	115.2k bps
Data bit length:	8 bit
Stop bit length:	1
Parity:	None
Flow control:	Yes

**3-3-1-2 HOST Command timing after cold start-up**

AT Commands that are used to control / configure the module may be issued when the “READY” result code has been received.

### 3-3-2 PCM

#### 3-3-2-1 Features

Bluetooth™ Module implements an audio transcoder to translate between A-law,  $\mu$ -law and linear voice data from the host and A-law,  $\mu$ -law and CVSD voice data over the air. Voice interpolation for lost packets is also included. PCM\_OUT, PCM\_IN, PCM\_CLK and PCM\_SYNC carry up to three bi-directional channels of voice data, each at 8ks/s. The format of the PCM samples can be 8-bit A-law, 8-bit  $\mu$ -law, 13-bit linear or 16-bit linear. The PCM\_CLK and PCM\_SYNC pins can be configured as inputs or outputs, depending on whether Bluetooth™ Module is the master or slave of the PCM interface.

PCM\_SYNC operates at a fixed clock frequency of 8kHz. When PCM\_SYNC is operated as an output (master mode) a clock frequency of 8kHz is generated from this pin. When operated as an input (slave mode) 8kHz must be input on this pin.

PCM\_CLK operates at a fixed clock frequency of 256kHz. When PCM\_CLK is operated as an output (master mode) a clock frequency of 256kHz is generated from this pin. When operated as an input (slave mode) 256kHz must be input on this pin.

When used with the Motorola MC145483 PCM or compatible devices, bits 1 to 13 of the PCM\_OUT data carry the current output sample value. Bits 14 to 16 carry a three-bit signals level value and these 'level bits' allow to vary the level of the audio signal output from the PCM device.

#### 3-3-2-2 Recommended codec IC

Bluetooth™ Module can be interfaced directly to appropriate PCM audio chips as below listed.

OKI MSM7705 four channel  $\mu$ /A-law codec

Motorola MC145481 8-bit  $\mu$ /A-law codec

Motorola MC145483SD 13-bit linear codec

Mitel MT93LI6 Echo canceling codec

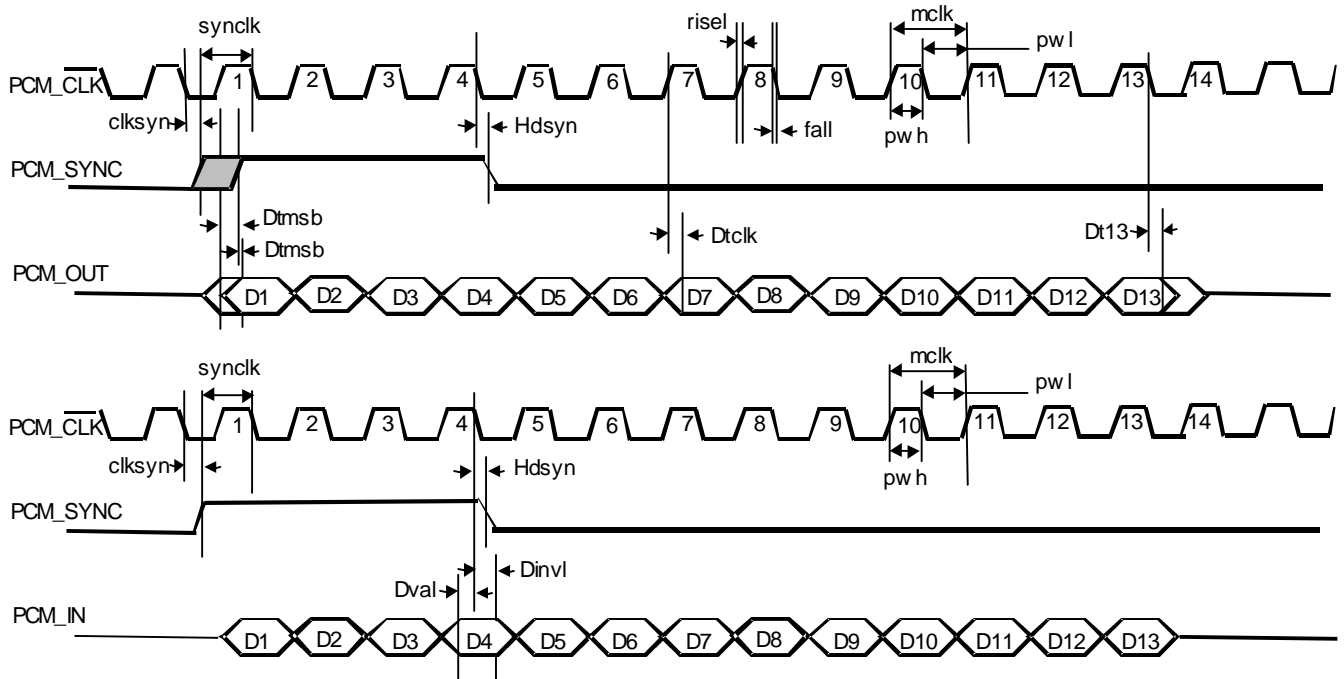
#### 3-3-2-3 PCM\_OUT and PCM\_IN 13 bit data format (based on Motorola MC145483SD)

PCM data stream is output from MSB in a sequential order, the following complement data format should be used for maximum positive code and negative zero and full scale.

Input / Output level	Sign bit	MSB											
+ Full scale	0	1	1	1	1	1	1	1	1	1	1	1	1
+One step	0	0	0	0	0	0	0	0	0	0	0	0	1
+0	0	0	0	0	0	0	0	0	0	0	0	0	0
-One step	1	1	1	1	1	1	1	1	1	1	1	1	1
-Full scale	1	0	0	0	0	0	0	0	0	0	0	1	0

### 3-3-2-4 Operating Condition Example (based on Motorola MC145483SD)

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V <sub>IH</sub>	Input High Voltage (PCM_CLK, SYNC, IN, PWRDWN)		VCC-0.5		VCC	V
V <sub>IL</sub>	Input Low Voltage (PCM_CLK, SYNC, IN, PWRDWN)		0		0.6	V
V <sub>OH</sub>	Output high voltage (PCM_CLK, SYNC, OUT)		2.2		VCC	V
V <sub>OL</sub>	Output low voltage (PCM_CLK, SYNC, OUT)		0		0.4	V
Mclk	Shift clock output (PCM_CLK)	at room temp	-20	256kHz	20	ppm
Sync	8khz sync clock (PCM_SYNC)	at room temp	-20	8kHz	20	ppm
Dc	Clock duty cycle ratio	at room temp	45	50	55	%
Pwh	Min pulse(High) width of PCM_CLK	See Fig	50			ns
Pwl	Min pulse width (Low) of PCM_CLK	See Fig	50			ns
Rise	Rising time for PCM signals	See Fig			50	ns
Fall	Falling time of PCM signals	See Fig			50	ns
Clksyn	Hold time form PCM_CLK (low) to PCM_SYNC (High)	See Fig	20			ns
Syncnk	Setup time form PCM_SYNC (High) to PCM_CLK (Low)	See Fig	80			ns
Hdsyn	Hold time from 4 <sup>th</sup> Period of PCM_CLK (Low) to PCM_SYNC (Low)	See Fig	50			ns
Dtmsb	Delay time from PCM_SYNC or PCM_CLK, Whichever later, to PCM_OUT for valid MSB data	See Fig			60	ns
Dtclk	Delay time from PCM_CLK Hi to PCM_OUT for valid data	See Fig			60	ns
Dt13	Delay time from later of 13 <sup>th</sup> PCM_CLK falling edge, or falling edge of PCM_SYNC to PCM_OUT to be High Z	See Fig			60	ns
Dval	Setup time PCM_IN valid to PCM_CLK (Low)	See Fig	0			ns
Dinv	Hold time PCM_CLK (Low) to PCM_IN invalid	See Fig	50			ns



### 4 PIN DESCRIPTION (refer to mechanical drawing for pin location)

Name	No	I/O	Description	Active state	Usage	Typical External Connection
						UART / PCM
GND	1	---	Ground		GND	GROUND
VCC	2	I	Main supply voltage input 1 Regulated DC source recommended	+3.3 V±0.1V	Power	De-coupling capacitor required <sup>1</sup>
VDD <sup>2</sup>	3	O	DC voltage monitor (+1.8V) when voltage regulator is integrated	+1.8V monitor	Power monitor	De-coupling capacitor required <sup>1,2</sup>
RESET	4	I	System Reset. (for test purpose)	Hi: Active (Reset) Lo: Inactive	RESET	Host CPU port or Vcc via capacitor
RF IN/OUT	5	I/O	RF input/output	---	RF IN/OUT	To the antenna
GND	6	---	Ground		GND	GROUND
SPI_CLK	7	I	Serial Peripheral Interface clock	Hi: 1 Lo: 0	SPI	SPI_CSB
MUM (PIO5)	8	O	Determines the type of information transmitted via UART.	Hi: Active	GPIO	Host CPU port
HUM (PIO3)	9	I	Determines the type of information received via UART	Hi: Active	GPIO	Host CPU port
SPI_CSB	10	I	Chip select for Synchronous Serial Interface	Hi: Inactive Lo: Active	SPI	SPI_CSB
SPI_MISO	11	O	Serial Peripheral Interface data output.	Hi: 1 Lo: 0	SPI	SPI_MISO
SPI_MOSI	12	I	Serial Peripheral Interface data input	Hi: 1 Lo: 0	SPI	SPI_MOSI
GND	13	---	Ground		GND	GROUND
PCM_CLK	14	I/O	Connection to PCM reference Clock input/output of 256kHz (No use for USB mode)	Hi: 1 Lo: 0	PCM	PCM Clock I/O (BCLKR, BCLKT, MCLK <sup>4</sup> ) or N.C. <sup>3</sup>
PCM_OUT	15	O	PCM data stream output (No use for USB mode)	Hi:1 Lo: 0	PCM	PCM input (DR <sup>4</sup> ) or N.C. <sup>3</sup>
PCM_SYNC	16	I/O	Connection to PCM frame sync Input/output of 8Khz (No use for USB mode)	Hi: Active Lo: Inactive	PCM	Frame Sync I/O (FST, FSR <sup>4</sup> ) or N.C. <sup>3</sup>
PCM_IN	17	I	PCM data stream input (No use for USB mode)	Hi:1 Lo: 0	PCM	PCM output (DT <sup>4</sup> ) or N.C. <sup>3</sup>
GND	18	---	Ground		GND	GROUND
UART_RxD	19	I	UART / RxD from DTE (No use for USB mode)	Hi:0 Lo:1	UART	TxD
UART_TxD	20	O	UART / TxD to DTE (No use for USB mode)	Hi:0 Lo:1	UART	RxD
UART_CTS	21	I	UART / Clear To Send from DTE (No use for USB mode)	Hi: De-assert Lo: Assert	UART	RTS
UART_RTS	22	O	UART / Ready To Send to DTE (No use for USB mode)	Hi: De-assert Lo: Assert	UART	CTS
N.C	23	---	No Connection		N.C	N.C.
N.C	24	---	No Connection		N.C	N.C.

Notes:

- <sup>1</sup>. In order to stabilize module performances, the below de-coupling capacitors would be required on application platform.  
VCC: 2.2μ~5.6μF Tantalum capacitor and 1000pF ~ 1μF ceramic capacitor  
VDD: 2.2μ~5.6μF Tantalum capacitor and 1000pF ~ 1μF ceramic capacitor
- <sup>2</sup>. Due to limited capacity of integrated voltage regulator, any load except de-coupling capacitors shall not be tied to this pin.
- <sup>3</sup>. Termination method if this pin is not used.
- <sup>4</sup>. Pin name is based on Motorola 13bit Linear PCM codec IC MC145483.

**5 DC CHARACTERISTIC (VCC = 3.3 V)**

Mode	Symbol	MIN	MAX	UNIT	PIN	CONDITION
Input HIGH level	V <sub>IH</sub>	VCCx0.8	VCC	V	**1	
Input LOW level	V <sub>IL</sub>	-0.4	+0.7	V	**1	
Output HIGH level	V <sub>OH</sub>	VCC-0.3	-----	V	**1	I <sub>OH</sub> =-200μA
Output LOW level	V <sub>OL</sub>	-----	+0.3	V	**1	I <sub>OL</sub> =200μA

Note:

- \*1. UART\_RTS, UART\_CTS, UART\_TXD, UART\_RXD, PCM\_IN, PCM\_SYNC, PCM\_OUT, PCM\_CLK, SPI\_CLK, SPI\_CSB, SPI\_MISO, SPI\_MOSI and RESET pins are relevant.

## 6 SOFTWARE SPECIFICATIONS

For the detail description of the implemented firmware, please refer to “Alps Embedded Audio Gateway Beta5 Firmware Release Note Document Version 1.0”.

### 6-1. Limitation of Liability

The built in firmware on this module shall be tested and verified by customer in combination with appropriate Bluetooth™ compliant upper layer protocol software on the actual application platform. Customer needs to verify the firmware functionality with the software as ALPS is only able to test the firmware in accordance with the Bluetooth™ Test Specification (Part C) and its internal testing procedures. After ALPS receives customer’s final agrees that ALPS shall not be liable or responsible for any damages or losses to module and/or customer’s application platform to the extent caused by the Verified Firmware. Customer assumes any and all risks associated with the use of the Verified Firmware and shall indemnify, defend, and hold ALPS harmless from third party claims arising from such use.

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<sup>1)</sup> Please visit [www.csr.com](http://www.csr.com) for such information.

## 7 MECHANICAL SPECIFICATIONS

### 7-1 General Mechanical Characteristics

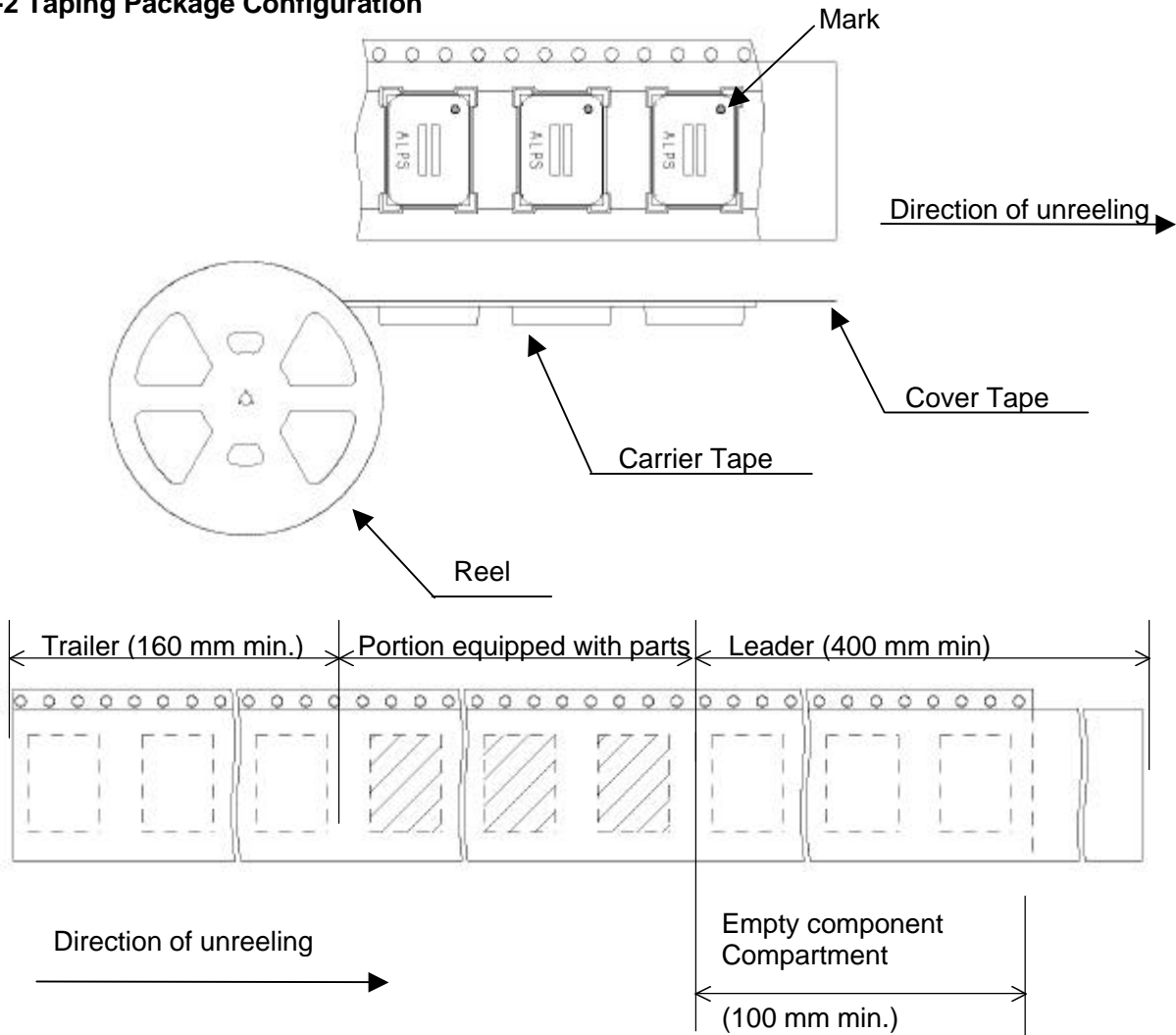
Aspect	No contamination No scratches No strains
Dimensions	13.5 x 10.0 x 2.1mm typ. (Refer to assembly drawing)
Weight	0.5g typ.
Composition of bump array solder	Sn-3.0Ag-0.5Cu

### 7-2 Taping Specification

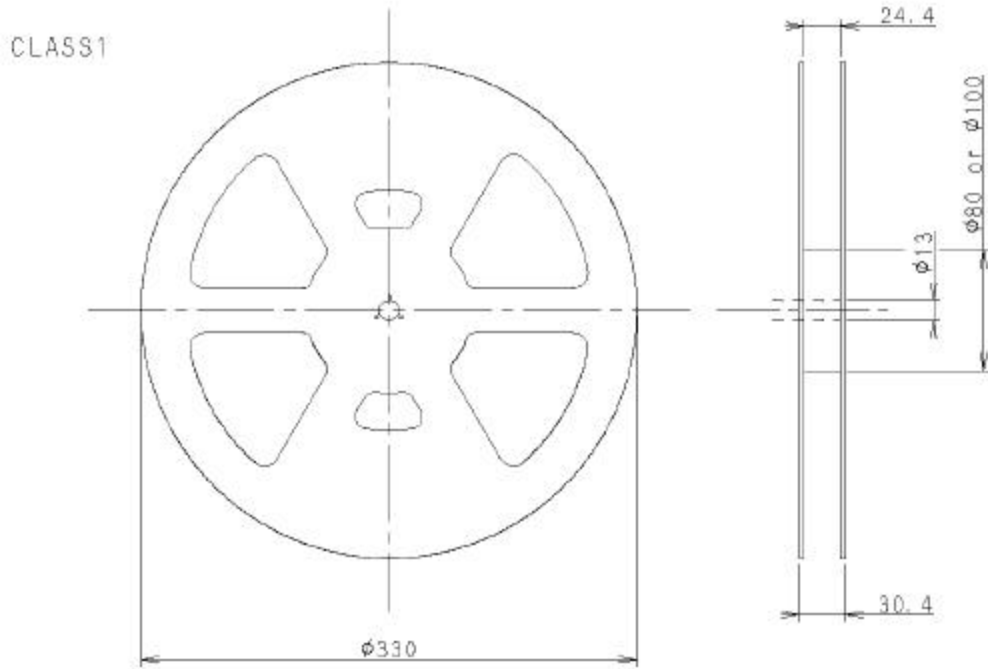
#### 7-2-1 Construction and Materials

Package type	Parts	Materials
Taping	Reel	PS or PPE or CARD BOARD
	Carrier Tape	Conductive PS or Conductive PPE or Conductive PP
	Cover Tape	PET

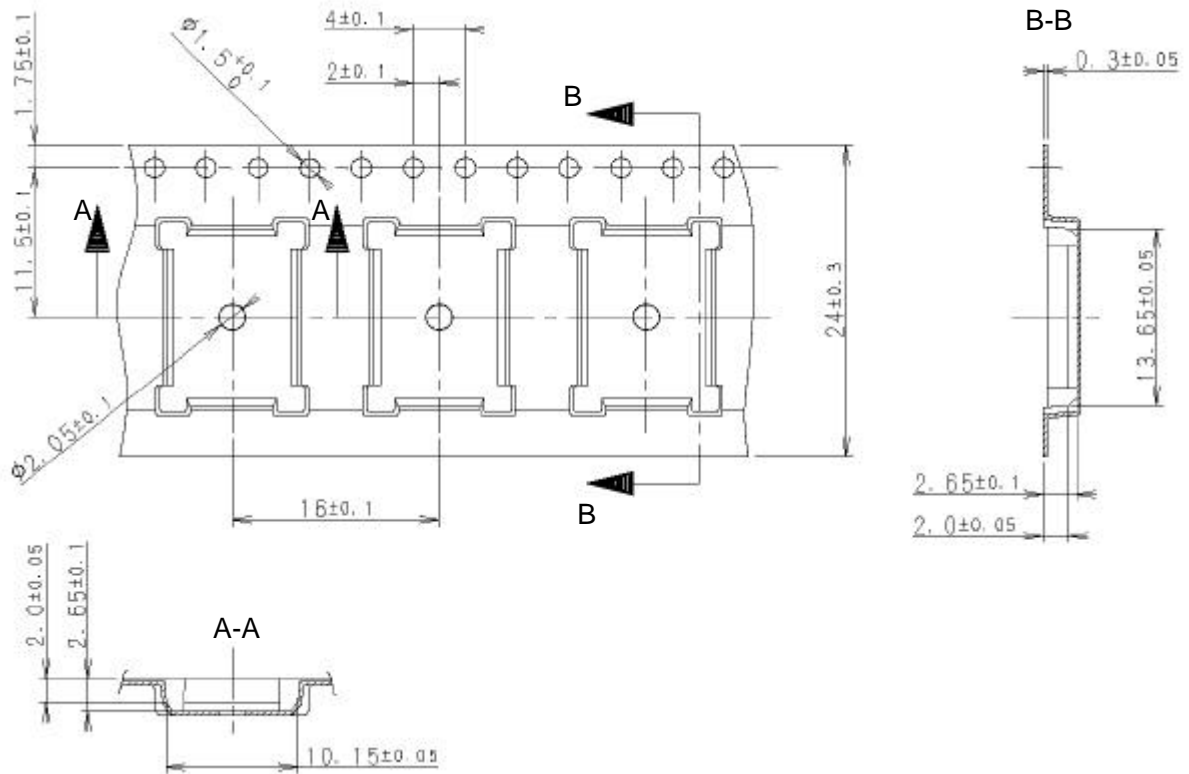
#### 7-2-2 Taping Package Configuration



**7-2-3 Reel Dimensions**

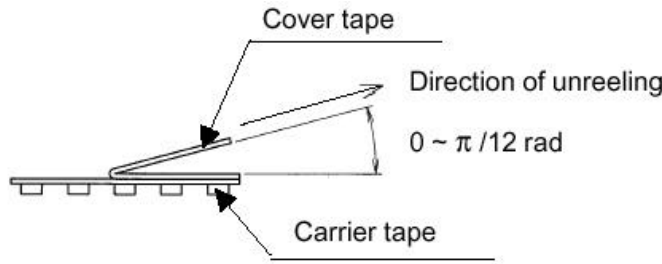


**7-2-4 Carrier Tape Dimensions**



**7-2-5 Characteristics of Carrier and Cover Tapes**

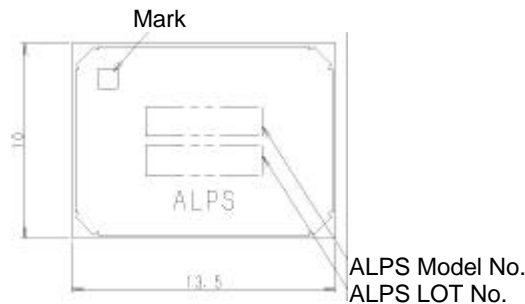
- 1) Peeling strength of cover tape.  
Peeling strength of cover tape shall be 0.1 N to 0.7 N and tested as follows.  
\*Peeling speed of cover tape shall be 300 mm / min.



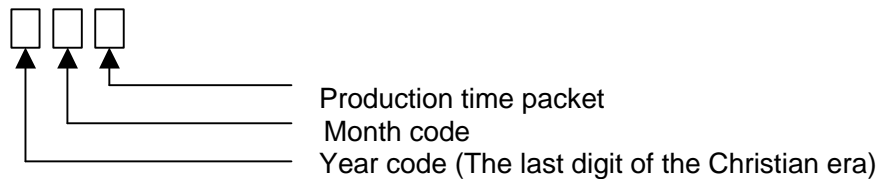
- 2) Cover tape shall not close the pilot holes or protrude from the carrier tape.
- 3) Minimum bending radius-taping package.  
Falling off of the Module or breakage of taping package shall not occur at minimum bending radius of 50 mm.
- 4) Strength of carrier tapes and covers tape  
Carrier tape: When a tensile force of 10 N is applied in the direction of unreeling of the tape, the tape shall withstand this force.  
Cover tape: When a tensile force 10 N is applied to the tape, the tape shall withstand this force.

**7-3 Marking Specifications**

Marking on the shield case of module contains the below contents.



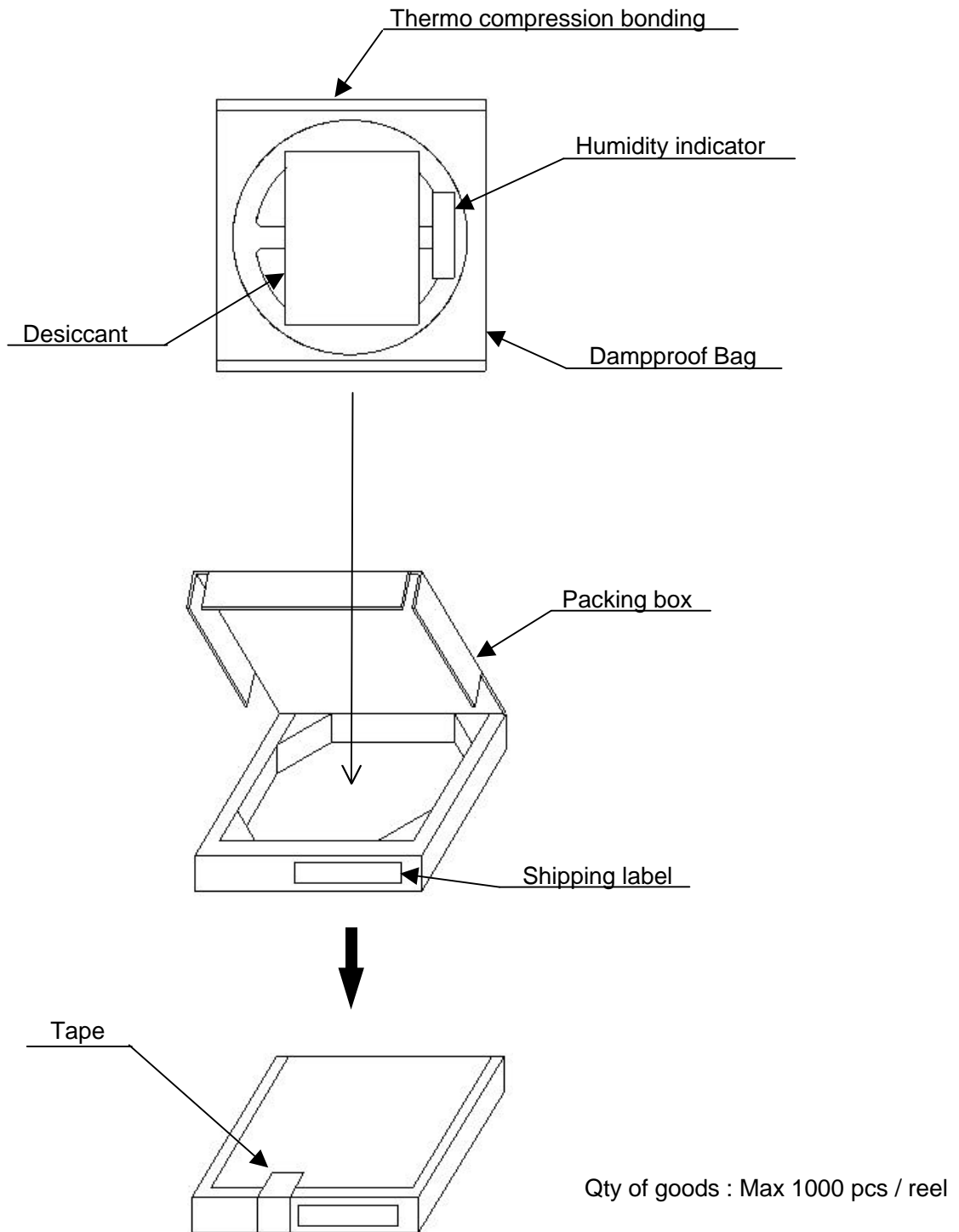
- 1) Mark: position of PIN No.1
- 2) ALPS Model No.: last 7 digits of ALPS model number are marked as follows;  
e.g.) ALPS model number: UGXZ5-□□□A  
Marking on shield case: Z1-□□□A
- 3) ALPS LOT No. : The LOT number contains 3 characters that are described as follows;



Note: the code of production month is specified according to the following table.

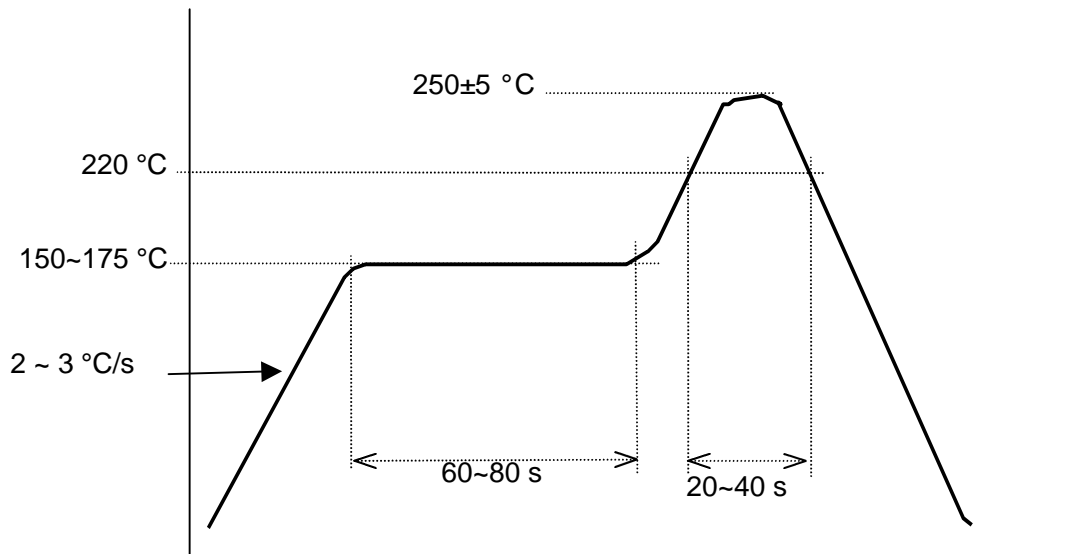
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**7-4 Packing Specifications**



### 7-5 Recommended Soldering Conditions

- 1) Heating method  
Conventional Convection or IR/Convection.
- 2) Temperature measurement  
Thermocouple d=0.1 mm ~ 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method.
- 3) Solder Paste composition  
Sn / 3.0Ag / 0.5Cu
- 4) Temperature profile  
Allowable reflow soldering times: 2 time based on the below reflow soldering profile



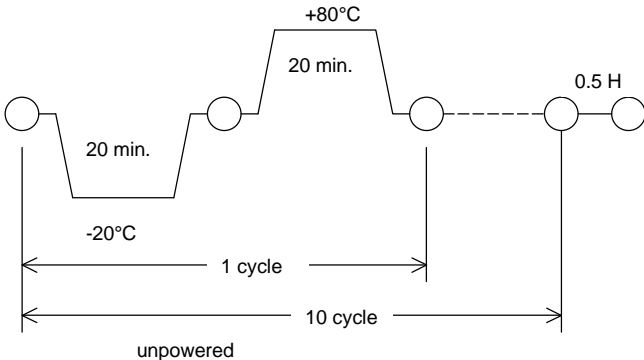
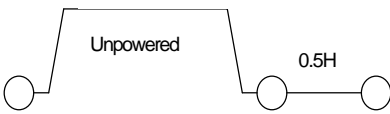




### 7-6 Attention to soldering and storage conditions

This product is subject to MSL4 according to EIA/J-STD-020A and -033.  
The following conditions shall be kept for soldering and keeping in storage this product.

1. Shelf life in dry bag: 6 months at 15 to 30 °C and < 75 % relative humidity (RH)
2. After dry bag is opened, module that will be subjected to soldering reflow or equivalent processing must be:
  - a) Mounted within 72 hours at factory condition of ≤30 °C / 60 % RH, or
  - b) Stored at < 20 % RH
3. Modules require baking, before mounting, if:
  - a) Humidity Indicator Card is >20 % when read at 23 °C ± 5 °C, or
  - b) Item 2.a) or 2.b) are not met
4. If baking is required, device may be baked for 192 hours at 40 °C +5 °C / -0 °C and < 5 % RH for low-temperature device containers

### 8 RELIABILITY TEST TEST METHOD

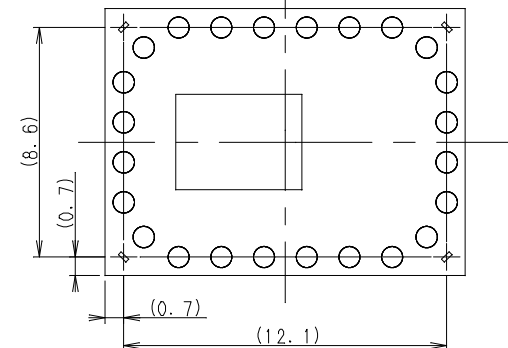
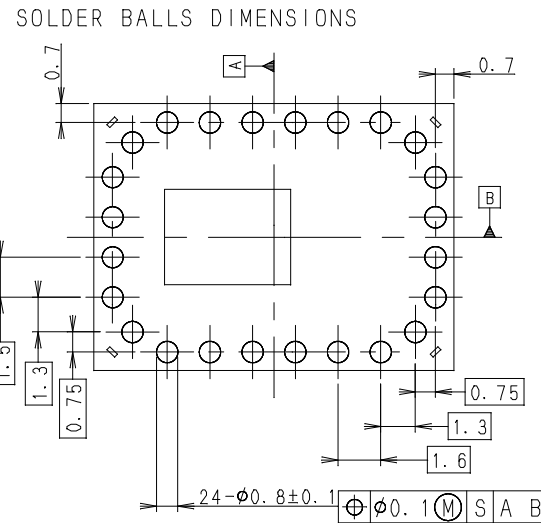
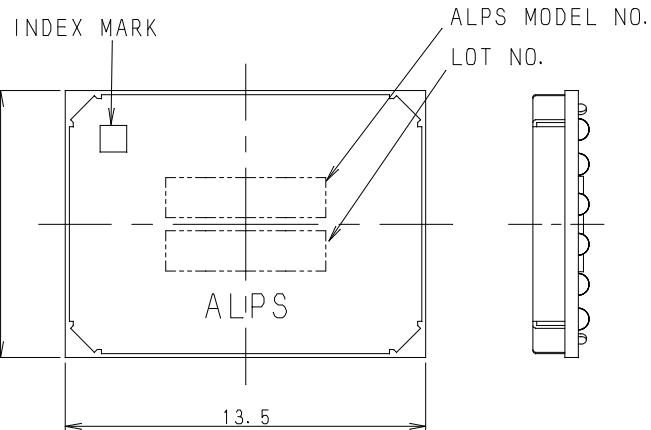
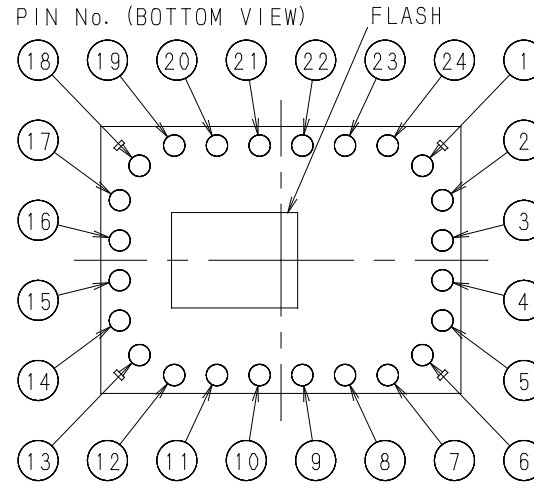
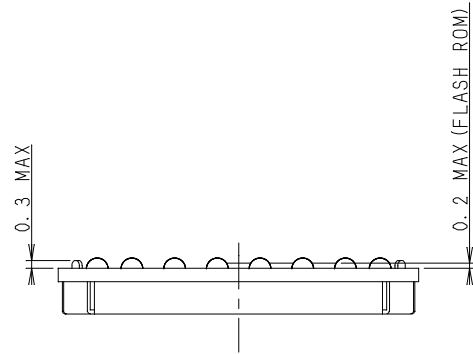
ITEM	Condition	Specification
High Temperature Test (No power applied)	85°C 96H 	Table 1
Temperature Test	-40°C 96H 	Table 1
Temperature Shock		Table 1
Humidity Test	40°C 90% 96H 	Table 1
Vibration Test	Vibration Frequency: 10 Hz, 55 Hz, 10 Hz (1 cycle / 1 minutes) Total Amplitude : 1 mm Direction : X, Y, Z (Each direction 40 minutes) 	Table 1
Drop Test	Drop Point (Height): 1 m Receiving board: Wooden board (20 x 20 x 3 cm.) Drop times: 1 times Direction: Any direction without the part of connector 	Table 1

**TABLE-1**

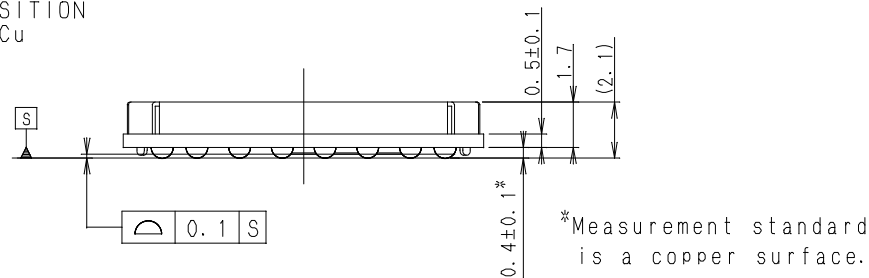
TX Frequency Accuracy	±75 kHz MAX.
Normal Transmitter Power	+20 dBm MAX. (Class1)
Input Sensitivity	-70 dBm MAX.

**Mechanical Drawing**

CONFIDENTIAL



24-SOLDER BALLS  
SOLDER COMPOSITION  
Sn/3.0Ag/0.5Cu



NOTE 1. TOLERANCES ARE ±0.3 UNLESS OTHERWISE SPECIFIED.  
2. LOT NO. SHALL BE CONFORMED TO ALPS ENDOWMENT RULES.

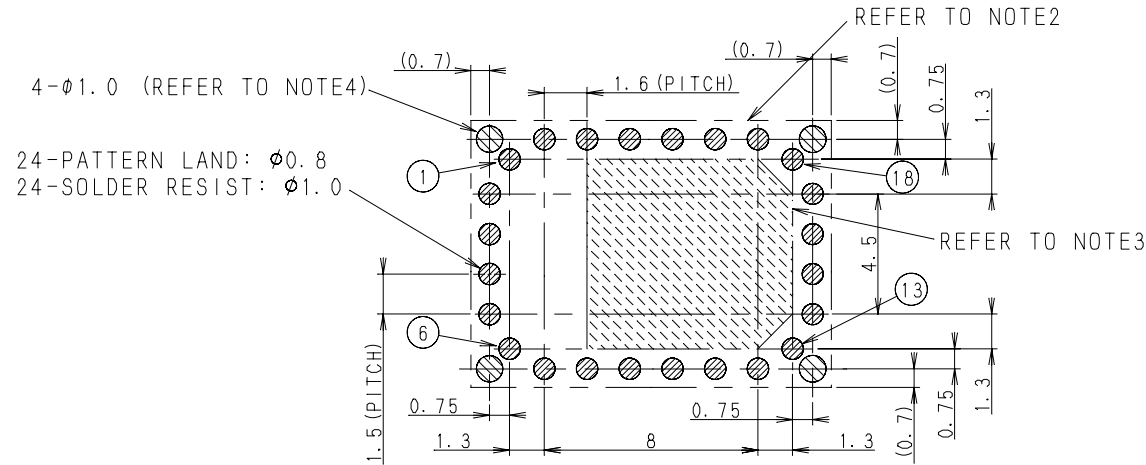
UGXZ5□□□□□  
CUSTOMER'S MODEL No. ALPS MODEL No.

PART NO.	NAME	MATERIAL	SPEC.	FINISH
		<b>ALPS ALPS ELECTRIC CO., LTD.</b>		
		DSGD. Oct. 14, '05 K. Terashima	SCALE 5 : 1	
		CHKD.	TITLE UGXZ5 ASSEMBLY DRAWING	
		APPD. Oct. 14, '05 H. Watanabe		UNIT mm
ZONE	SYMB.	DATE OR NO.	APPD.	CHKD.

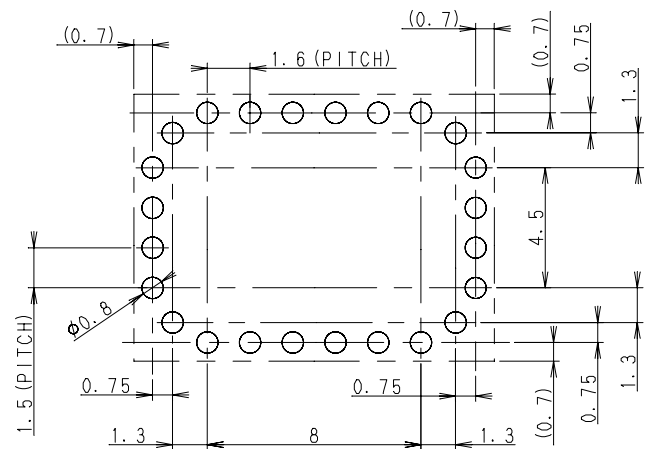
PRELIMINARY

CONFIDENTIAL

RECOMMENDED PAD DIMENSIONS FOR MOUNTING MODULE



METAL MASK DIMENSIONS (t=0.1mm)



- NOTE 1. TOLERANCES ARE ±0.1 UNLESS OTHERWISE SPECIFIED.
- 2. ANY COMPONENTS SHALL NOT BE PLACED IN THIS AREA. (UNDER MODULE)
- 3. ANY PATTERNS SHALL NOT BE PLACED IN THIS AREA.
- 4. INHIBITED AREA FOR PATTERN LAND. (GND PATTERN IS EXCLUDED)

	UGXZ5-□□□□
CUST. MODEL NO.	ALPS MODEL NO.

PART NO.	NAME	MATERIAL	SPEC.	FINISH
		<b>ALPS ALPS ELECTRIC CO., LTD.</b>		
		DSGD.	SCALE	
		Oct. 19, '04 K. Terashima	5 : 1	
		CHKD.	⊕	TITLE
		APPD.		PAD RECOMMENDATION
ZONE	SYMB.	DATE OR NO.	APPD.	UNIT
			Oct. 19, '04 H. Watanabe	mm